Location	Job Title	Responsibilities	Requirements	Degree Qualification
Edinburgh	Database Research	The Database team within the Huawei Edinburgh Research Centre researches and develops	Required:	PhD is preferred but not
	Engineer	next generation transactional and analytical data management systems for Huawei and	Have a solid computer science background.	essential
	(Graduate Scheme)	Huawei devices. As such, we are looking to recruit people with experience or interest in one	Be comfortable with research methodology.	
	(Internship available)	or more of: query planning and optimisation, query execution engines, data storage and indexing engines, concurrency control mechanisms, hardware-software co-design,	Be comfortable with system design and implementation. Be data-driven.	
		concurrent/parallel algorithms and data structures, distributed and/or decentralised systems	Be proficient in one or more system-level programming languages (C/C++, Rust,	
		and protocols, benchmarking and performance analysis, and programming/query languages	etc.).	
		and compilers. Key Responsibilities:	Be proficient in one or more of the areas specified in above Job Summary. Have participated in the implementation of (aspects of) a database management	
		Perform systems research and empirical science on current and future data management	system or systems of a similar low-level nature (e.g., operating systems, compilers	
		and processing systems.	etc.).	
		Analyse and understand requirements for the next generation of database storage and query	Desired:	
		 processing engines. Design, implement, and deploy key technical building blocks for the next generation of data 	 Have published papers at top peer-reviewed conferences or journals in fields related to the above (desired but not essential). 	
		management and processing systems.	inc above (desired but not essential).	
C.I. 1	C . I C	•Explore and advance the latest data management and processing frameworks for both	n : 1	NID: C II .
Edinburgh	System Infrastructure Research Engineer	 Contribute to the research and development team's exploration of emerging technologies and systems. 	Required: -Bachelors or Master's degree in Computer Science or a related technical field.	PhD is preferred but not essential
	(Graduate Scheme)	Engage in team projects to conduct system design, analysis, and prototype development.	Be comfortable with research methodology.	
	(Internship available)	•Play a role in selecting research problems, designing solutions, analysing results, and	*Be comfortable with system design and implementation.	
		building prototypes to showcase the advantages and challenges of these technologies across various data center and cloud applications.	 Have an in-depth understanding of operating systems and/or distributed systems and/or cloud computing. 	
		Design, implement, and evaluate key technologies and associated algorithms.	•Good programming skills, master of at least one language, such as C/C++, Go,	
		Actively engage with academia, industry, and open-source communities to establish	Python etc.	
		influence and contribute to the broader technological landscape.	•Good communication and teamworking skills. Desired:	
			•PhD in operating systems, distributed systems etc.	
			Published papers in top journals/conferences.	
Ipswich	R&D Design &	Develop R&D test rig prototypes (HW & SW) & test methodology	•Recent PhD in physics or Engineering	PhD is preferred but not
	Verification Engineer	•DC and RF verification testing/characterisation of early stage development devices and prepare and publish technical reports of finding/proposed improvements	Experience in optoelectronic device characterisation, DC and RF Familiarity with software used for automated testing	essential
		Plan, develop & execute project-based test strategy Plan, develop & execute project-based test strategy	Excellent data analysis and report writing skills	
		 Engage with Design team to discuss and analyse specifications and define test plans. 	<u> </u>	
	1	Engage with supplier to buy off-the-shelf/customised solution to fit project requirements Transfer test methodology to Backend team & support them during NPI phase		
Ipswich	Process Engineer	Contribute to the process development roadmap to ensure that process capability and	Experience with Process equipment and associated metrology tools.	PhD is preferred but not
	1	toolset stays at the forefront of technology and enables the product roadmap	 Track record in using structured problem-solving techniques. 	essential
		Day to day operation owner of a defined process tool set. Direct techniques (operators to process P & D and manufacturing wafers to meet schedules).	•Master's Degree in relevant subject, Physics, Chemistry, Material Science, Chemical	
		Direct technicians/operators to process R&D and manufacturing wafers to meet schedules. Develop, modify, and continuously improve manufacturing process and procedures to	Engineering, Electronic Engineering etc. •Knowledge and experience of SPC processes.	
	1	enable higher productivity, reduced scrap, and improved quality.		
		 Setup and monitoring statistical process and control (SPC) charts. 		
		•Assist in creating building blocks within process modules.		
		 Applying various statistical methods to improve reproducibility and manufacturability through Failure Mode Effect Analysis (FMEA), Control Plan and Gage R&R studies. 		
		Document tool operation and process details and write standard of procedures (SOPs)		
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Ipswich	Test and Software Engineer	Support & develop photonics test and measurement software Support & develop data & results extraction reports software	Graduate or experienced software developer Software languages & development environment skills - C++, C#, Visual Studio	PhD is preferred but not essential
	z.iigiiieu	Produce clean, efficient code based on project and user requirements	Agile software development practices & source version controls	Continui
		Verify and deploy version-controlled release packages	Candidate must possess good verbal and written communication skills	
		Troubleshoot, debug and upgrade existing software & tools	Python, Labview, SQL DB design and build	
		Create technical documentation for reference and reporting Communicate and build software specifications based on customer requirements.		
		Provide professional levels of support to end users		
Ipswich	Photonic PIC Design	Design and/or contribute to the development of Photonic integrated circuits and discrete	PhD in a relevant semiconductor/material or device design topic;	PhD is preferred but not
	Engineer	active photonic III-V components Optoelectronic device design, in particular device mask design and waveguide/optical	Knowledge of III-V optoelectronic device physics Experience in Mask design/PDKs, TCAD software, Python/Nazca/Klayout or	essential
		modelling.	Equivalent	
			Experience of commercial optical waveguide software packages	
		•Engage with Design and Fabrication team to discuss and analyse specifications and define		
		mask set requirements and PDKs; automate the implementation of design rules.	Excellent data analysis and report writing skills	
			Excellent data analysis and report writing skills	
		mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *DC and RP verification of early stage development devices and prepare and publish	*Excellent data analysis and report writing skills	
Cambridge	Graduate CDLI Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PDC and RF verification of early stage development devices and prepare and publish technical reports of finding/proposed improvements		Phd or Postgraduate
Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *DC and RP verification of early stage development devices and prepare and publish	*Excellent data analysis and report writing skills *PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains	Phd or Postgraduate
Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PC and RF verification of early stage development devices and prepare and publish *technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture	Phd or Postgraduate
Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *DC and RF verification of early stage development devices and prepare and publish technical reports of finding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling	Phd or Postgraduate
Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PC and RF verification of early stage development devices and prepare and publish *technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture	Phd or Postgraduate
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Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PtC technology *PC and RF verification of early stage development devices and prepare and publish technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM,	Phd or Postgraduate
Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *DC and RF verification of early stage development devices and prepare and publish technical reports of finding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming	Phd or Postgraduate
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Cambridge	Graduate CPU Architect	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PC and RF verification of early stage development devices and prepare and publish *echnical reports of finding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and personal specification may be reviewed on an ongoing basis in accordance with the changing needs of Huawei Research and Development	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectXII or 12 and/or OpenCL	Phd or Postgraduate
	Graduate CPU Architect Al Processor Software &	mask set requirements and PDKs; automate the implementation of design rules. Support external collaborative projects with Academic and Industrial institutions. Fexplore and analyse new directions for future applications of PIC technology. PDC and RF verification of early stage development devices and prepare and publish technical reports of Inding/proposed improvements. Identifying CPU bottleneck via workload and CPU performance analysis. CPU functional and performance modelling to help CPU architecture exploration. Identifying the key missing technologies in the current architecture. Contributing to design & research methodologies to increase the efficiency and effectiveness. This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and perviewed on an	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of ArmRISC-V assembly languages Facellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies Knowledge NN technologies HopenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies HopenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies HopenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies HopenGLES, Metal, DirectX11 or 12 and/or OpenCL	-
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	AI Processor Software & Hardware Co-design	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PC and RF verification of early stage development devices and prepare and publish technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture **Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by this/her line manager. The job description and personal specification may be reviewed on an ongoing basis in accordance with the changing needs of Huawei Research and Development UK Limited. *Be responsible for one of the sub technical direction of AI Processor Software & Hardware Co-design Lab, identify key root technologies related to NPU chips, develop evolution strategies and moadmaps, promote and implement the evolution strategies to build industry- leading technical competitiveness, support Huawei's business success in the computing field. *Carry out technology and business innovation, integrate several sub-domains of applications algorithms, frameworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architectures competitiveness. *Grasp the AI industry and technology trends, gain insight into the development direction of AI applications and resolve key usability and performance issues in full-stack AI through	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86, RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies Kich experience in optimizing AI chip architectures and AI systems, be familiar with mainstream heterogeneous computing software and hardware architectures in the industry, and have comprehensive capabilities from applications to basic software to chips. Hands-on experience of one of the following technologies: Numerical Calculation, Compilation, Algorithm & chip co-design, Runtime, Shared Memory. Knowledge of AI industry application scenarios, be familiar with mainstream models and algorithm development trends, and be able to extract requirements for the chip layer. Proficient in key bottlenecks identification based on scenarios such as NLP and large models and key application algorithms to drive reasonable software architecture	-
Cambridge Cambridge	AI Processor Software & Hardware Co-design	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PC and RF verification of early stage development devices and prepare and publish technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and personal specification may be reviewed on an ongoing basis in accordance with the changing needs of Huawei Research and Development UK Limited. *Be responsible for one of the sub technical direction of AI Processor Software & Hardware *Co-design Lab, identify key root technologies related to NPU chips, develop evolution strategies and roadmaps, promote and implement the evolution strategies to build industry-leading technical competitiveness, support Huawei's business success in the computing field. *Carry out technology and business innovation, integrate several sub-domains of application algorithms, frameworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architectures of basic AI software and applications and algorithms, edvelop key technical architectures of basic AI software and applications and algorithms.	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectXII or 12 and/or OpenCL Knowledge NN technologies Rich experience in optimizing AI chip architectures and AI systems, be familiar with mainstream heterogeneous computing software and hardware architectures in the industry, and have comprehensive capabilities from applications to basic software to chips. Hands-on experience of one of the following technologies: Numerical Calculation, Compilation, Algorithm & chip co-design, Runtime, Shared Memory. Knowledge of AI industry application sscenarios, be familiar with mainstream models and algorithm development trends, and be able to extract requirements for the chip layer. Proficient in key bottlenecks identification based on scenarios such as NLP and large models and key application algorithms to drive reasonable software architecture evolution.	-
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Cambridge	AI Processor Software & Hardware Co-design Engineer Graduate-CPU/NPU Performance Modelling	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *PDC and RF verification of early stage development devices and prepare and publish *technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and personal specification may be reviewed on an angoing basis in accordance with the changing needs of Huawei Research and Development UK Limited. *Be responsible for one of the sub technical direction of AI Processor Software & Hardware *Co-design Lab, identify key root technologies related to NPU chips, develop evolution strategies and roadmaps, promote and implement the evolution strategies to build industry- leading technical competitiveness, support Huawei's business success in the computing field. *Carry out technology and business innovation, integrate several sub-domains of application algorithms, frameworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architecture competitiveness. *Carry to ut technology services, span and the development direction of AI applications and algorithms, develop key technical architectures of basic AI software and hardware, and resolve key usability and performance issues in full-stack AI through technical projects.	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Good knowledge of Arm/RISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies Rich experience in optimizing AI chip architectures and AI systems, be familiar with mainstream heterogeneous computing software and hardware architectures in the industry, and have comprehensive capabilities from applications to basic software to chips. Hands-on experience of one of the following technologies: Numerical Calculation, Compilation, Algorithm & chip co-design, Runtime, Shared Memory. *Knowledge of AI industry application scenarios, be familiar with mainstream models and algorithm development trends, and be able to extract requirements for the chip layer. Proficient in key bottlenecks identification based on scenarios such as NLP and large models and key application algorithms to drive reasonable software architecture evolution. Desired: Experience in software usability improvement projects. *Relevant experience in several sub-fields of AI application algorithms, frameworks, runtime, modelling and simulation, and compilers. *In-depth understanding of the innovative methods, platforms, and tools of AI head manufacturers, and have experience in transforming application and academic research achievements into commercial products. *Proficient bedeeping and wising performance simulators like GEM5 (O3 model), *Proficient bedeeping and vising performance simulators like GEM5 (O3 model), *Proficient bedeeping and vising performance simulators like GEM5 (O3 model), *Proficient bedeeping and vising performance simulators like GEM5 (O3 model), *Proficient bedeeping and vising performance s	Phd or Postgraduate
Cambridge	AI Processor Software & Hardware Co-design Engineer	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PC technology *PC and RF verification of early stage development devices and prepare and publish *technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *CPU intentional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and personal specification may be reviewed on an ongoing basis in accordance with the changing needs of Huawei Research and Development UK Limited. *Be responsible for one of the sub technical direction of AI Processor Software & Hardware Co-design Lab, identify key root technologies related to NPU chips, develop evolution strategies and roadmaps, promote and implement the evolution strategies to build industry- leading technical competitiveness, support Huawei's business success in the computing field. *Carry out technology and business innovation, integrate several sub-domains of application algorithms, frameworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architecture competitiveness. Grasp the AI industry and technology trends, gain insight into the development direction of AI applications and algorithms, farmeworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architecture competiti	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of ArmRISC-V assembly languages Good knowledge of ArmRISC-V assembly languages Excellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies Rich experience in optimizing AI chip architectures and AI systems, be familiar with mainstream theregeneous computing software and hardware architectures in the industry, and have comprehensive capabilities from applications to basic software to chips. Knowledge Of AI industry application socenarios, be familiar with mainstream therefore the comprehensive capabilities from applications to basic software to chips. Knowledge of AI industry application socenarios, be familiar with mainstream models and algorithm development trends, and be able to extract requirements for the chip layer. Proficient in key bottlenecks identification based on scenarios such as NLP and large models and key application algorithms to drive reasonable software architecture evolution. Desired: Experience in software usability improvement projects. Relevant experience in several sub-fields of AI application algorithms, frameworks, runtime, modelling and simulation, and compilers. 1-n-depth understanding of the innovative methods, platforms, and tools of AI head manufacturers, and have experience in transforming application and academic research achievements into commercial products. Profound background in workload modelling and CPU architecture Experience in developing and using performance simulators like GEM5 (O3 model), Sniper or others	Phd or Postgraduate
Cambridge	AI Processor Software & Hardware Co-design Engineer Graduate-CPU/NPU Performance Modelling	mask set requirements and PDKs; automate the implementation of design rules. *Support external collaborative projects with Academic and Industrial institutions *Explore and analyse new directions for future applications of PIC technology *DC and RF verification of early stage development devices and prepare and publish technical reports of Inding/proposed improvements *Identifying CPU bottleneck via workload and CPU performance analysis *CPU functional and performance modelling to help CPU architecture exploration *Identifying the key missing technologies in the current architecture exploration *Identifying the key missing technologies in the current architecture *Contributing to design & research methodologies to increase the efficiency and effectiveness This job description is only an outline of the tasks, responsibilities and outcomes required of the role. The jobholder will carry out any other duties as may be reasonably required by his/her line manager. The job description and personal specification may be reviewed on an ongoing basis in accordance with the changing needs of Huawei Research and Development UK Limited. *Be responsible for one of the sub technical direction of AI Processor Software & Hardware Co-design Lab, identify key root technologies related to NPU chips, develop evolution strategies and roadmaps, promote and implement the evolution strategies to build industry- leading technical competitiveness, support Huawei's business success in the computing field. *Carry out technology and business innovation, integrate several sub-domains of application algorithms, frameworks, runtime, modelling and simulation, and compilers from the perspective of processors, and build end-to-end architecture competitiveness. *Grasp the AI industry and technology trends, gain insight into the development direction of AI applications and algorithms, develop key technical architectures of basic AI software and hardware, and resolve key usability and performance issues in full-stack AI	PhD degree in Computer Science, Electrical & Electronic Engineering, Computer Architecture or related domains Good knowledge of CPU architecture Experience in CPU modelling Good knowledge of Arm/RISC-V assembly languages Facellent in C/C++ programming Familiar with at least one of the ISAs: ARM, X86. RISC-V, MIPS, ARC Desired: Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL Knowledge NN technologies Rich experience in optimizing AI chip architectures and AI systems, be familiar with mainstream heterogeneous computing software and hardware architectures in the industry, and have comprehensive capabilities from applications to basic software to chips. Hands-on experience of one of the following technologies: Numerical Calculation, Compilation, Algorithm & chip co-design, Runtime, Shared Memory. Knowledge of AI industry application scenarios, be familiar with mainstream models and algorithm development trends, and be able to extract requirements for the chip layer. Proficient in key bottlenecks identification based on scenarios such as NLP and large models and key application algorithms to drive reasonable software architecture evolution. Desired: Experience in software usability improvement projects. Relevant experience in several sub-fields of AI application algorithms, frameworks, runtime, modelling and simulation, and compilers. In-depth understanding of the innovative methods, platforms, and tools of AI head manufacturers, and have experience in transforme in transforming application and academic research achievements into commercial products. Profound background in workload modelling and CPU architecture Experience in developing and using performance simulators like GEM5 (O3 model), Sniper or others	Phd or Postgraduate
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PU			
	General algorithm and architectural feature research Madelling and simulation.	Required: PhD in relevant discipline	Phd or Postgraduate
	2. Modelling and simulation		
	5. Performance/Power Tuning	Self-motivated, well organized and good	
		team player	
		Good verbal and writing communication	
		skill, great coding skill	
		. Desired:	
		Hands-on experience with one or more of the following technologies: Vulkan.	
LMs(Large Language	· Carry out a literature review and investigate the state-of-the-art frameworks and models.	Successful candidates should be/have	Phd or Postgraduate
odels) Researcher	· Work on solving important challenges and conduct cutting-edge research in LLMs.	· Creative and innovative.	_
-	· Build benchmarks/baselines using public datasets.	· Able to convert an idea into a prototype efficiently, optimize its cost and drive the	
	· Finetune LLMs on novel, applicable and practical tasks.	implementation.	
	Model evaluation and refinement.	· Excellent knowledge of existing LLMs.	
	 Publish research papers at top-tier NLP/ML/AI conferences and journals. 		
	1 1 1		
L	Ms(Large Language	Searcher 3. Feature and micro-architecture implementation trade-off 4. Real-time graphics algorithms or shader program design and optimization to improve performance, save bandwidth and power 5. Performance/Power Tuning Ms(Large Language dels) Researcher - Carry out a literature review and investigate the state-of-the-art frameworks and models. - Work on solving important challenges and conduct cutting-edge research in LLMs. - Build benchmark/baselines using public datasets. - Firentume LLMs on novel, applicable and practical tasks.	3. Feature and micro-architecture implementation trade-off. 4. Real-time graphics algorithms or shader program design and optimization to improve performance, save bandwidth and power 5. Performance/Power Tuning 5. Performance/Power Tuning 6. Good verbal and writing communication skill, great coding skill 7. Desired: 8. Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL 8. Knowledge NR technologies 8. Self-motivated, well organized and good team player 9. Good verbal and writing communication skill, great coding skill 9. Desired: 9. Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL 9. Knowledge NR technologies 8. Work on solving important challenges and conduct cutting-edge research in LLMs. 9. Build benchmarks/baselines using public datasets. 1. Firetune LLMs on novel, applicable and practical tasks. 1. Model evaluation and refinement. 1. Excellent knowledge of at least one of, graphics APIs and pipelines, GPU architectures, GPU computing, modelling and simulation, ray tracing or compiler technologies 9. Self-motivated, well organized and good team player 1. Good verbal and writing communication skill, great coding skill 1. Desiruct: 1. Hands-on experience with one or more of the following technologies: Vulkan, OpenGLES, Metal, DirectX11 or 12 and/or OpenCL 1. Knowledge NR technologies 1. Work on solving important challenges and conduct cutting-edge research in LLMs. 1. Self-motivated, well organized and good team player 1. Good verbal and writing communication skill, great coding skill 1. Desiruct. 1. Hands-on experience with one or more of the following technologies: 1. Valuation of creative and important challenges and models. 2. Carry out a literature review and investigate the state-of-the-art frameworks and models. 2. Carry out a literature review and investigate the state-of-the-art frameworks and models. 2. Carry out a literature rev